Notice of Allowability	Application No.	Applicant(s)	
	10/695,267	ROSS ET AL.	
	Examiner	Art Unit	
	DIEM K. CAO	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed on 2/11/2008 and Interview on 5/20/2008*.

2. ☒ The allowed claim(s) is/are *1,4,6-8,11,13-18, now renumbered 1-12*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20080521* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Robert Bergstrom (Reg. No. 39,906) on May 20, 2008.

2. The claims have been amended as follows:

Please replace all the existing claims with the following claims.

Claim 1. A computer processor that executes instructions and that supports virtual machine monitor operation and implementation, the computer processor comprising:

a virtualization-mode processor state for execution of non-virtual-machine-monitor instructions;

a non-virtualization-mode processor state for execution of virtual machine monitor instructions; and

a virtualization-mode-switch instruction that

before switching from one mode to another, checks to ensure that page attributes of a virtual memory page containing the virtualization-mode-switch instruction are compatible with the virtualization-mode-switch instruction,

when executed by a process running in virtualization mode, checks to ensure that a current priority level is a most privileged virtualized priority level before switching from

virtualization mode to non-virtualization mode, without incurring an interruption, to enable execution of one ore more virtual machine monitor instructions; and

when executed by a process running in non-virtualization mode, checks to ensure that the current priority level is a highest priority level before switching from non-virtualization mode to virtualization mode without incurring an interruption.

Claim 2 (Canceled)

Claim 3 (Canceled)

Claim 4. A computer processor that executes instructions and that supports virtual machine monitor operation and implementation, the computer processor including:

a virtualization-mode processor state for execution of non-virtual-machine-monitor instructions;

a non-virtualization-mode processor state for execution of virtual machine monitor instructions; and

a virtualization fault invoked by the computer processor when a routine executing in virtualization mode at a highest privilege level attempts to execute an instruction needing virtualization, the virtualization fault having a lower priority than improper-instruction-related faults, so that an associated virtualization-fault handler in a computer system including the computer processor can avoid emulating improper-instruction-related faults.

Claim 5 (Canceled)

Claim 6. The computer processor of claim 4 wherein the processor is switched to non-virtualization mode when the virtualization fault is triggered by the computer processor.

Claim 7. A computer processor that executes instructions and that supports virtual machine monitor operation and implementation, the computer processor including

a virtualization-mode processor state for execution of non-virtual-machine-monitor instructions;

a non-virtualization-mode processor state for execution of virtual machine monitor instructions; and

a flexible highest-implemented-virtual-address bit that, in virtualization mode, is checked by the processor and reported by the virtual machine monitor to be less than the highest-implemented-virtual-address bit in non-virtualization mode, so that a high-order portion of virtual-address space is accessible only to a virtual machine monitor executing in non-virtualization mode, while a low-order portion of virtual-address space is accessible to both the virtual machine monitor executing in non-virtualization mode and to one or more processes executing in virtualization mode.

Claim 8. A method for enhancing a computer processor to support virtual-machine-monitor operation and implementation, the method comprising:

to a computer processor that executes instructions and that provides registers, adding

a virtualization-mode processor state for execution of non-virtual-machine-monitor instructions;

a non-virtualization-mode processor state for execution of virtual machine monitor instructions; and

a virtualization-mode-switch instruction that

before switching from one more to another, checks to ensure that page attributes of a virtual memory page containing the virtualization-mode-switch instruction are compatible with the virtualization-mode-switch instruction,

when executed by a process running in virtualization mode, checks to ensure that a current priority level is a most privileged virtualized priority level before switching from virtualization mode to non-virtualization mode, without incurring an interruption, to enable execution of one ore more virtual machine monitor instructions; and

when executed by a process running in non-virtualization mode, checks to ensure that the current priority level is a highest priority level before switching from non-virtualization mode to virtualization mode without incurring an interruption.

Claim 9 (Canceled)

Claim 10 (Canceled)

Claim 11. A method for enhancing a computer processor to support virtual-machine-monitor operation and implementation, the method comprising:

to a computer processor that executes instructions and that provides registers, adding

a virtualization-mode processor state for execution of non-virtual-machine-monitor instructions;

a non-virtualization-mode processor state for execution of virtual machine monitor instructions; and

a virtualization fault invoked by the computer processor when a routine executing in virtualization mode at a highest privilege level attempts to execute an instruction needing virtualization, the virtualization fault having a lower priority than improper-instruction-related faults, so that an associated virtualization-fault handler in a computer system including the computer processor can avoid emulating improper-instruction-related faults.

Claim 13. The method of claim 11 further comprising switching the processor to non-virtualization mode when the virtualization fault is triggered by the computer processor.

Claim 14. A method for enhancing a computer processor to support virtual-machine-monitor operation and implementation, the method comprising:

to a computer processor that executes instructions and that provides registers, adding

a virtualization-mode processor state for execution of non-virtual-machine-monitor instructions;

a non-virtualization-mode processor state for execution of virtual machine monitor instructions; and

a flexible highest-implemented-virtual-address bit that, in virtualization mode, is checked by the processor and reported by the virtual machine monitor to be less than the highest-implemented-virtual-address bit in non-virtualization mode, so that a high-order portion of virtual-address space is accessible only to a virtual machine monitor executing in non-virtualization mode, while a low-order portion of virtual-address space is accessible to both the virtual machine monitor executing in non-virtualization mode and to one or more processes executing in virtualization mode.

Claim 15. A method for supporting multiple, concurrent guest operating systems in a computer system, the method comprising:

providing a virtual-mode bit flag in a processor of the computer system;

providing a virtualization-mode-switch (*vmsw)* instruction in the processor that changes the state of the virtualization-mode bit flag to enable a guest operating system to directly enter virtual-machine-monitor mode without incurring an interruption;

providing a virtualization fault with an interruption vector, assigned to have a relatively low interruption priority, that is generated when a routine, executing at high priority in virtualization mode, attempts to execute a privileged instruction or an instruction that needs software virtualization assistance and that is associated with a virtualization fault handler; and

providing a virtual-machine monitor that executes privileged instructions on behalf of guest operating systems and provides to each guest operating system a virtual machine interface, the virtual-machine monitor invoked by *vmsw* instructions or a virtualization fault.

Claim 16. The method of claim 15 wherein address space is reserved for exclusive use by the virtual-machine monitor.

Claim 17. The method of claim 16 wherein the address space reserved for exclusive use by the virtual-machine monitor is addressed by addresses including a highest bit of implemented virtual address space, the virtual-machine monitor reporting a smaller implemented address space to guest operating systems addressed by addresses that do not include the highest bit of implemented virtual address space.

Claim 18. A computer-readable medium encoded with computer instructions that implement a method for supporting multiple, concurrent guest operating systems in a computer system, the method comprising:

providing a virtual-mode bit flag in a processor of the computer system;

providing a virtualization-mode-switch (*vmsw)* instruction in the processor that changes the state of the virtualization-mode bit flag to enable a guest operating system to directly enter virtual-machine-monitor mode without incurring an interruption;

providing a virtualization fault with an interruption vector, assigned to have a relatively low interruption priority, that is generated when a routine, executing at high priority in virtualization mode, attempts to execute a privileged instruction or an instruction that needs software virtualization assistance and that is associated with a virtualization fault handler; and

providing a virtual-machine monitor that executes privileged instructions on behalf of guest operating systems and provides to each guest operating system a virtual machine interface, the virtual-machine monitor invoked by *vmsw* instructions or a virtualization fault.

Claim 19 (Canceled)

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DIEM K. CAO whose telephone number is (571)272-3760. The examiner can normally be reached on Monday - Friday, 7:30AM - 3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195